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# Claims

[c1] 1.An all-in-one polishing process for a semiconductor wafer, the semiconductor wafer being positioned on a polishing platen of a chemical mechanical polishing (CMP) device and comprising a top surface, a bottom surface and an edge bevel surface, the edge bevel surface comprising a front side bevel, a backside bevel and an edge, the top surface comprising at least a first material layer, the edge bevel surface comprising a second material layer, the polishing process comprising:
performing a surface CMP process by utilizing a polishing pad to remove the first material layer on the top surface to a first thickness;
performing a rim CMP process to completely remove the second material layer on the front side bevel, the backside bevel and the edge;
performing a first cleaning process to clean the top surface, the front side bevel, the backside bevel, the edge, and the surface of the semiconductor wafer; and
drying the semiconductor wafer.

[c2] 2.The polishing process of claim 1 wherein either the first material layer or the second material layer com-

prises either a dielectric layer or a metal layer.

[c3] 3.The polishing process of claim 1 wherein either the first material layer or the second material layer is formed by performing either a chemical vapor deposition (CVD) process or an electric copper plating (ECP) process.

[c4] 4.The polishing process of claim 1 wherein the surface CMP process and the rim CMP process are performed by utilizing slurry.

[c5] 5.The polishing process of claim 4 wherein the rim CMP process is performed by utilizing at least one front side bevel pad, at least one backside bevel pad and at least one edge pad to polish and completely remove portions of the second material layer respectively on the front side bevel, the backside bevel and the edge of the semiconductor wafer.

[c6] 6.The polishing process of claim 4 wherein a second cleaning process is performed after the surface CMP process to clean the top surface of the semiconductor wafer.

[c7] 7.The polishing process of claim 6 wherein the first and second cleaning processes are performed by utilizing deionized water (DI water) to remove the residual slurry on the semiconductor wafer and flakes of the first and

second material layers respectively on the top surface and the edge bevel surface of the semiconductor wafer.

[c8] 8.The polishing process of claim 7 wherein a buffing polishing process is performed after the performance of the second cleaning process by utilizing a buffing pad.

[c9] 9.An all-in-one apparatus for polishing a semiconductor wafer, the semiconductor wafer comprising a top surface, a bottom surface and an edge bevel surface, the edge bevel surface comprising a front side bevel, a backside bevel and an edge, the top surface comprising at least one first material layer, the edge bevel surface comprising a second material layer, the apparatus comprising:

a polishing platen;

a wafer stage for containing the semiconductor wafer;

a polishing pad for polishing the first material layer on the top surface to a first thickness;

a notch pad for locating the coordination of the semiconductor wafer on the wafer stage;

a plurality of rollers for fixing the semiconductor wafer on the wafer stage;

at least one front side bevel pad for completely removing portions of the second material layer on the front side bevel;

at least one backside bevel pad for completely removing

portions of the second material layer on the backside bevel;

at least one edge pad for completely removing portions of the second material layer on the edge;

at least one slurry supply tube for providing slurry on the semiconductor wafer, the buffing pad, the front side bevel pad, the backside bevel pad and the edge pad; and

at least one cleaning solution supply tube for providing a cleaning solution for cleaning the semiconductor wafer.

[c10] 10.The all-in-one apparatus of claim 9 wherein the edge of the semiconductor wafer comprises a notch for engaging with the notch pad to locate the coordination of the semiconductor wafer on the wafer stage.

[c11] 11.The all-in-one apparatus of claim 9 wherein either the first material layer or the second material layer comprises either a dielectric layer or a metal layer.

[c12] 12.The all-in-one apparatus of claim 9 wherein either the first material layer or the second material layer is formed by performing either a CVD process or an ECP process.

[c13] 13.The all-in-one apparatus of claim 9 wherein the cleaning solution is DI water for removing the slurry on the semiconductor wafer and flakes of the first and sec-

ond material layers respectively on the top surface and the edge bevel surface of the semiconductor wafer.

[c14] 14.The all-in-one apparatus of claim 9 wherein the all-in-one apparatus comprises a buffing pad for performing a buffing polishing process on the top surface of the semiconductor wafer.

[c15] 15.An all-in-one polishing process for a semiconductor wafer, the semiconductor wafer being positioned on a polishing platen of a CMP device and comprising a top surface, a bottom surface and an edge bevel surface, the edge bevel surface comprising a front side bevel, a backside bevel and an edge, the top surface comprising at least one first material layer, the edge bevel surface comprising a second material layer, the edge comprising a notch for engaging with a notch pad of the CMP device to locate the coordination of the semiconductor wafer on the wafer stage, the polishing process comprising:
performing a rim CMP process to completely remove the second material layer on the front side bevel, the backside bevel and the edge;
performing a first cleaning process to clean the top surface, the front side bevel, the backside bevel and the edge of the semiconductor wafer; and
drying the semiconductor wafer.

[c16] 16.The polishing process of claim 15 wherein either the first material layer or the second material layer comprises either a dielectric layer or a metal layer.

[c17] 17.The polishing process of claim 15 wherein either the first material layer or the second material layer is formed by performing either a CVD process or an ECP process.

[c18] 18.The polishing process of claim 15 wherein slurry is mployed to perform a surface CMP process by utilizing a buffing pad of the CMP device to remove the first material layer on the top surface to a first thickness before performing the rim CMP process, and a second cleaning process is performed by utilizing DI water to clean the top surface of the semiconductor wafer after performing the surface CMP process.

[c19] 19.The polishing process of claim 18 wherein a buffing polishing process is performed on the top surface of the semiconductor wafer after the performance of the second cleaning solution by utilizing a buffing pad.

[c20] 20.The polishing process of claim 15 wherein slurry is employed to perform a surface CMP process by utilizing a buffing pad of the CMP device to remove the first material layer on the top surface to a first thickness after performing the rim CMP process, and a second cleaning

process is performed by utilizing DI water to clean the top surface of the semiconductor wafer after performing the surface CMP process.

[c21] 21.The polishing process of claim 20 wherein a buffing polishing process is performed on the top surface of the semiconductor wafer after the performance of the second cleaning solution by utilizing a buffing pad.

[c22] 22.The polishing process of claim 15 wherein the rim CMP process is performed by utilizing at least one front side bevel pad, at least one backside bevel pad and at least one edge pad to polish and completely remove portions of the second material layer respectively on the front side bevel, the backside bevel and the edge of the semiconductor wafer.

[c23] 23.The polishing process of claim 22 wherein the rim CMP process is performed by utilizing slurry and the CMP device.

[c24] 24.The polishing process of claim 23 wherein the EBR process is performed by utilizing DI water to remove the residual slurry and flakes of the second material layer on the edge bevel surface of the semiconductor wafer after the rim CMP process is performed.